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NUCLEAR INSTRUMENTATION FOR SCINTILLATION AND SEMICONDUCTOR SPECTROSCOPY

T.L. EMMER

ABSTRACT

This is a manual for those who use or service the newly developed transistorized instruments for nuclear spectroscopy: the Transistor Amplifier-- Double Line (TADL, Q-2205); the Snip-Snap Single-Channel Analyzer; the Fast Coincidence Unit; and the Biased Amplifier and Linear Gate. A general description is given for each instrument along with the specifications, a description of the circuit, and a procedure for initial testing.

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1.0 TRANSISTOR AMPLIFIER -- DOUBLE LINE (TADL)

1.1 General Description

The TADL, a linear pulse amplifier using double, delay-line clipping (Figs. 1.11 and 1.12), can be used with either scintillation counters or semiconductor detectors by using the proper preamplifier. Preamplifier power is supplied through the signal cable, which is the only cable required.

With three feedback-amplifier groups and two delay-line compensators (of the differential-amplifier type, each having a gain of 1), the amplifier has a total gain of 560 (Fig. 1.13). To prevent excessive overloading, each feedback-amplifier group is preceded by a limiter. The output, normally terminated in 100 ohms, is linear to ± 10 v.

A double-regulated power supply increases stability and reduces noise.

1.2 Specifications

1. Gain: 560 with a binary, 32-to-1 step attenuator (coarse gain) and a continuous, 2-to-1 fine gain.

2. Output: 0- to ± 10-v into 100 ohm termination.

3. Input: 0- to 4-v maximum negative pulse having greater than 50-μsec decay time.

4. Integral Nonlinearity: ± 0.2% (see Fig. 1.21).

5. Gain Stability: 0.03%/°F (see Fig. 1.22); and 0.12% per 10% change in line voltage.

6. Recovery Time: less than 12μ sec for 200X overload (see Fig. 1.23).

7. Counting Rate Limitations: see Fig. 1.24.

8. Resolution and Noise: 10μ v for the scintillation preamplifier; and 26 kev with no external input capacity for the semiconductor detector preamplifier (see Figs. 1.25, 1.26, and 1.27).

1.3 Circuit Description (Q-2205-1)

Negative input pulses from the preamplifier are clipped by the first, shorted delay line and applied to the base of Q1. The unclipped input pulses are attenuated by R8 and R9 and applied to the emitter of Q1. The

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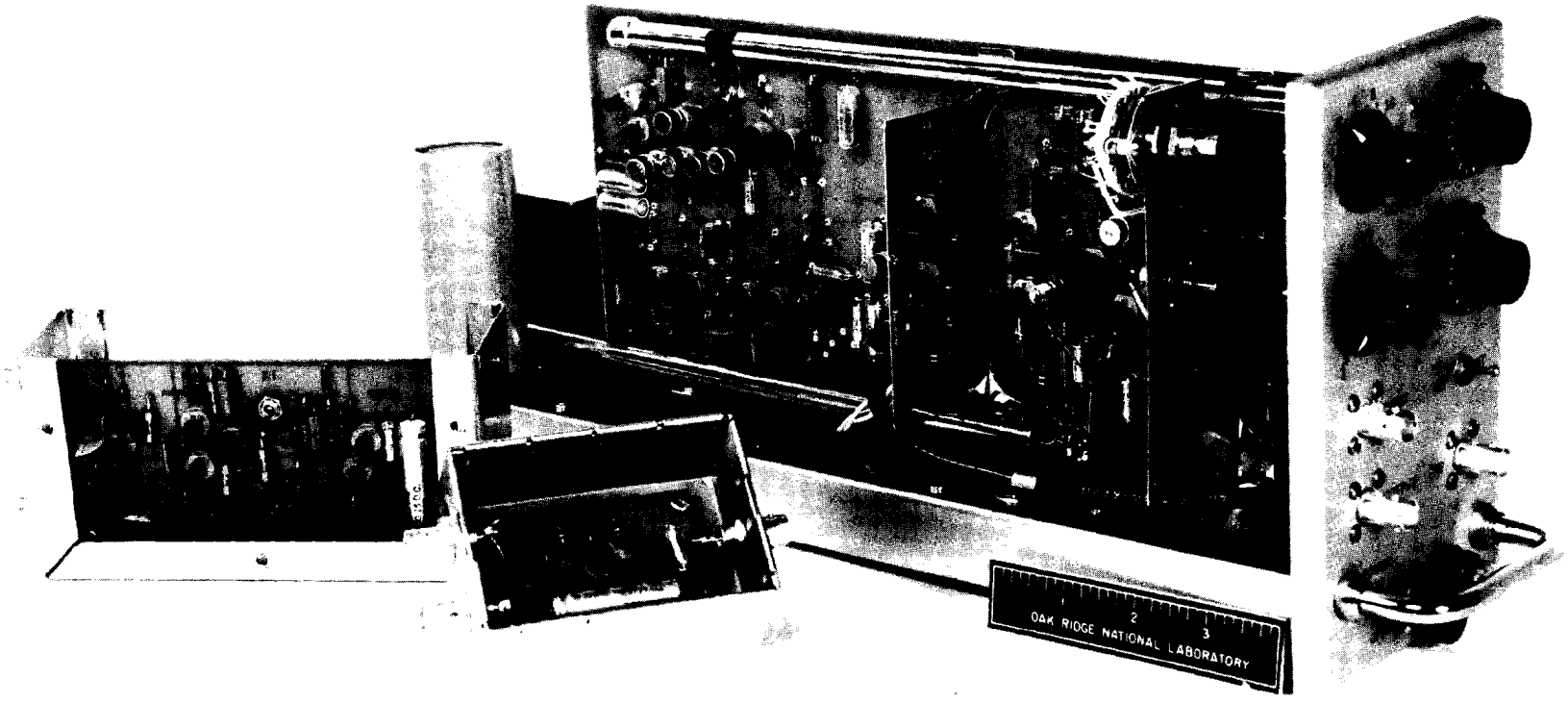


Fig. 1.11. TADL Amplifier, a Scintillation Preamplifier, a Semiconductor Detector Preamplifier, and a Snip-Snap Single-Channel Analyzer Chassis.

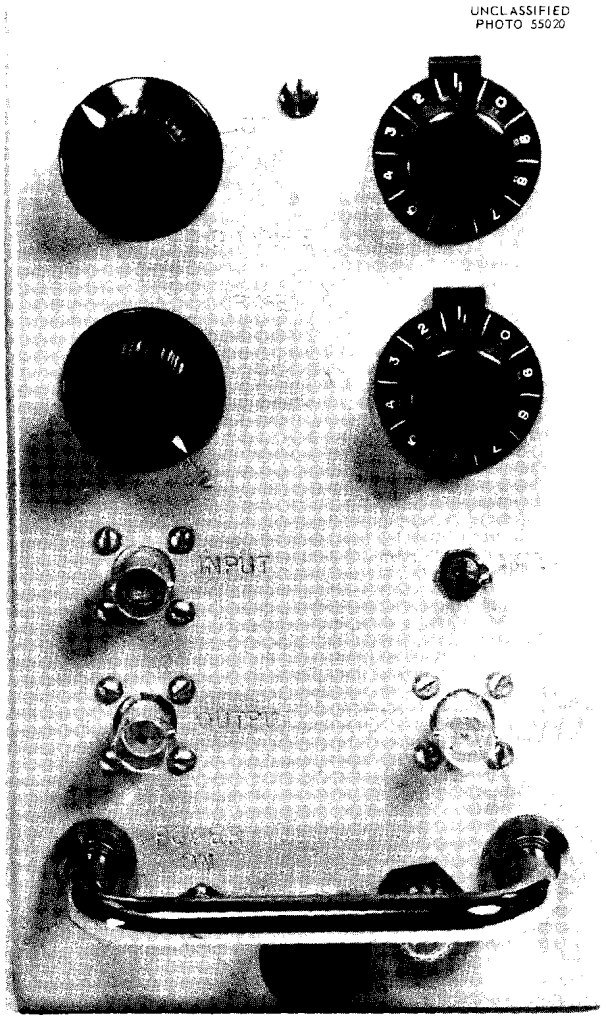


Fig. 1.12. Front Panel for a TADL Amplifier and a Snip-Snap Single-Channel Analyzer.

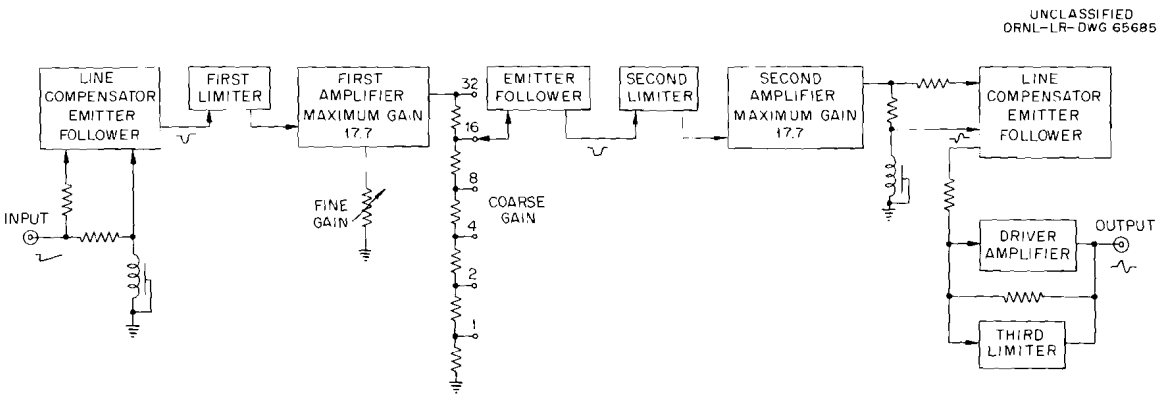


Fig. 1.13. Block Diagram of the Transistor Amplifier — Double Line.

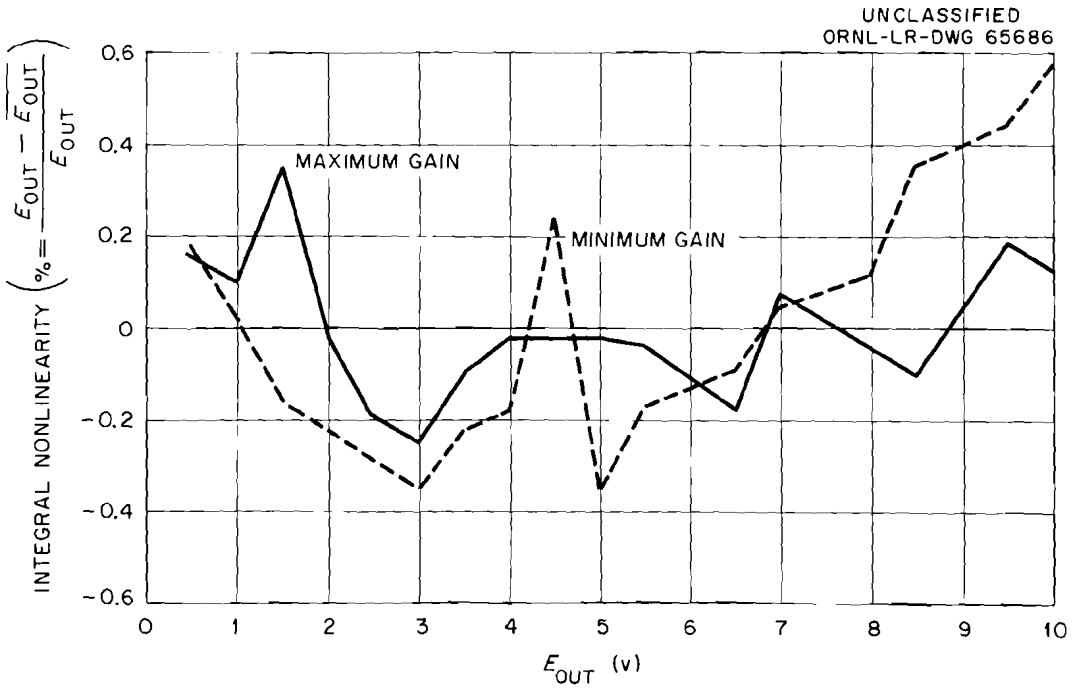


Fig. 1.21. Integral Nonlinearity of the Transistor Amplifier — Double Line.

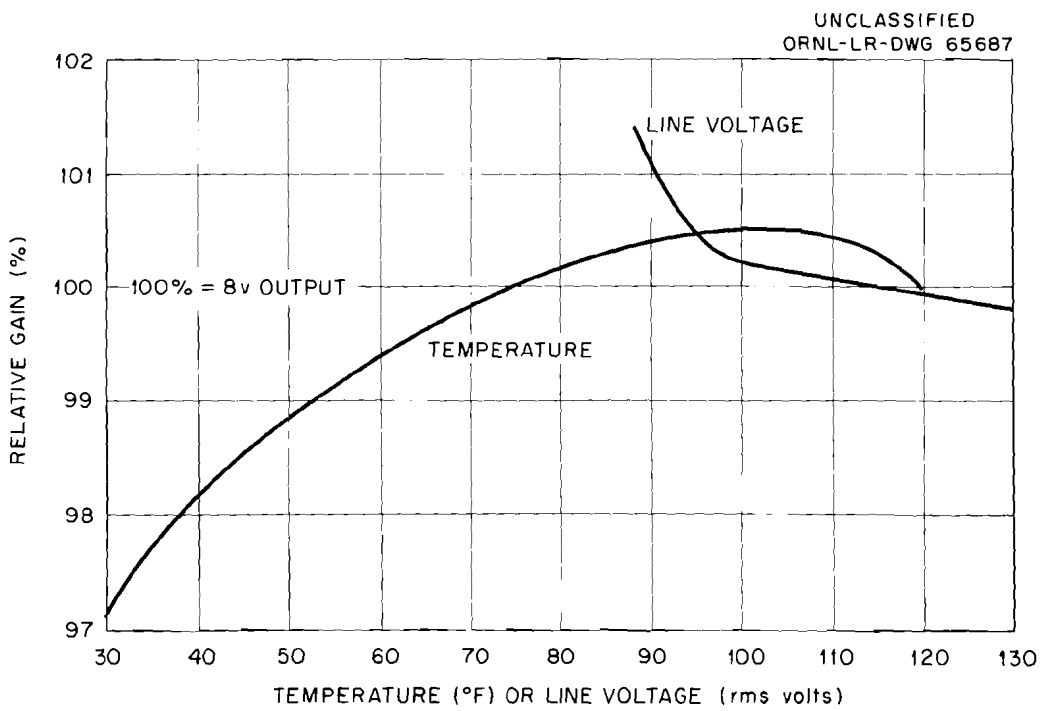


Fig. 1.22. Gain Stability of the Transistor Amplifier — Double Line with Changes in Temperature and Line Voltage.

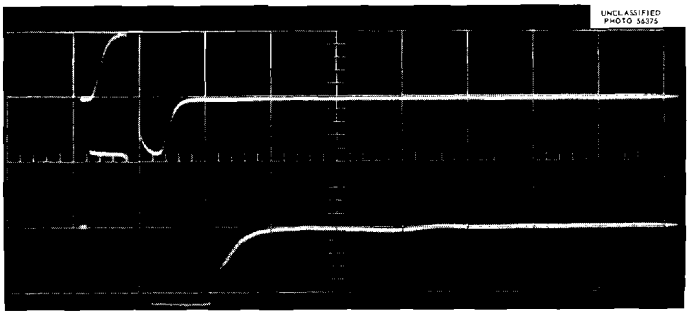


Fig. 1.23. Oscillogram Showing the Overload Characteristics of a Transistor Amplifier – Double Line. The top wave shows x1 overload and the bottom wave shows x200 overload. The horizontal scale is 1 μsec/cm and the vertical scale is 10 v/cm.

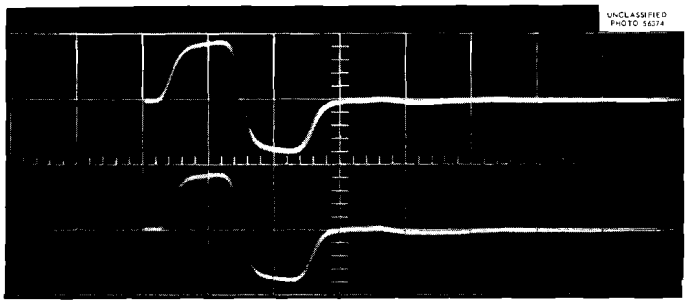


Fig. 1.24. Oscillogram Showing Counting Rate Limitations of the Transistor Amplifier – Double Line. The top wave shows pulses from a mercury pulser which have been amplified by a TADL. The bottom wave shows the same pulses with 10^5 counts/sec from Co^{60} background, 50% in overload. The horizontal scale is 1 μsec/cm and the vertical scale is 10 v/cm.

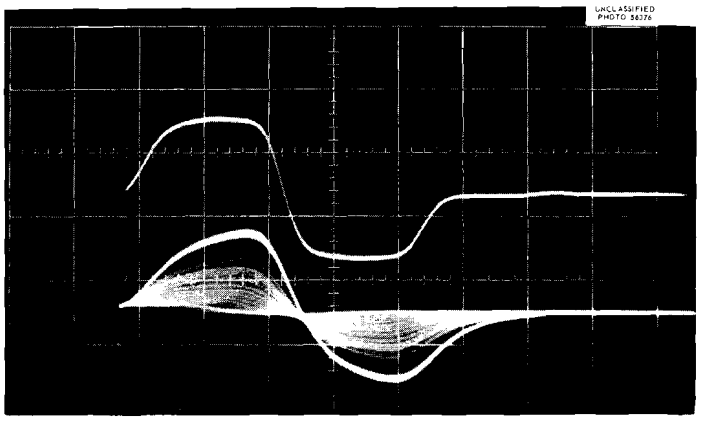


Fig. 1.25. Oscillogram Showing, at the Top, Spectrum of Gamma Rays from Cs^{137} and, at the Bottom, Spectrum of Alpha Particles from Po^{210}. The horizontal scale is 0.5 μsec/cm and the vertical scale is 5 v/cm.

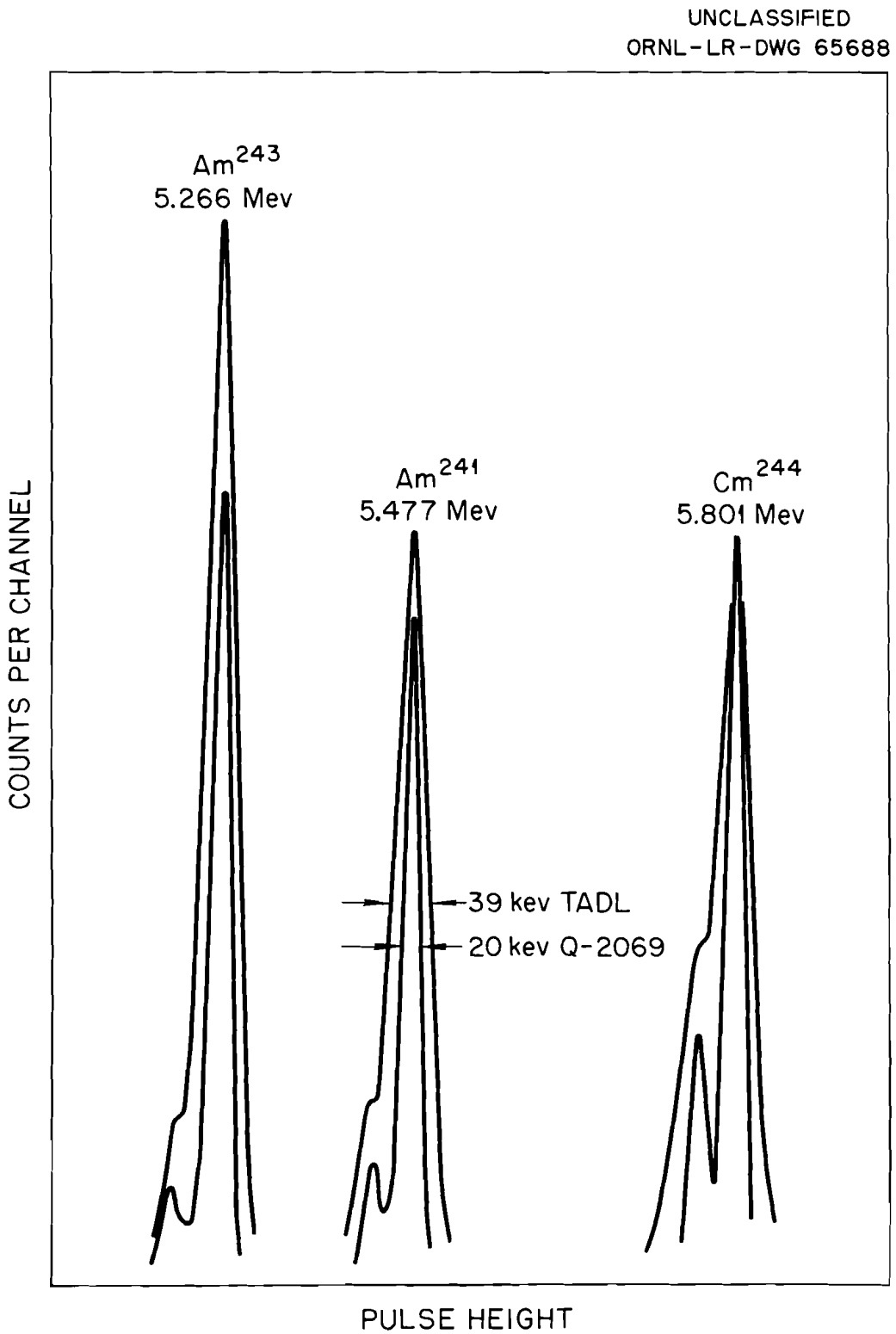


Fig. 1.26. Alpha-Particle Resolution of the TADL-1 and Q-2069 Amplifier Using a 16-mm^2 Au-Si Surface Barrier Detector with 200-v Bias.

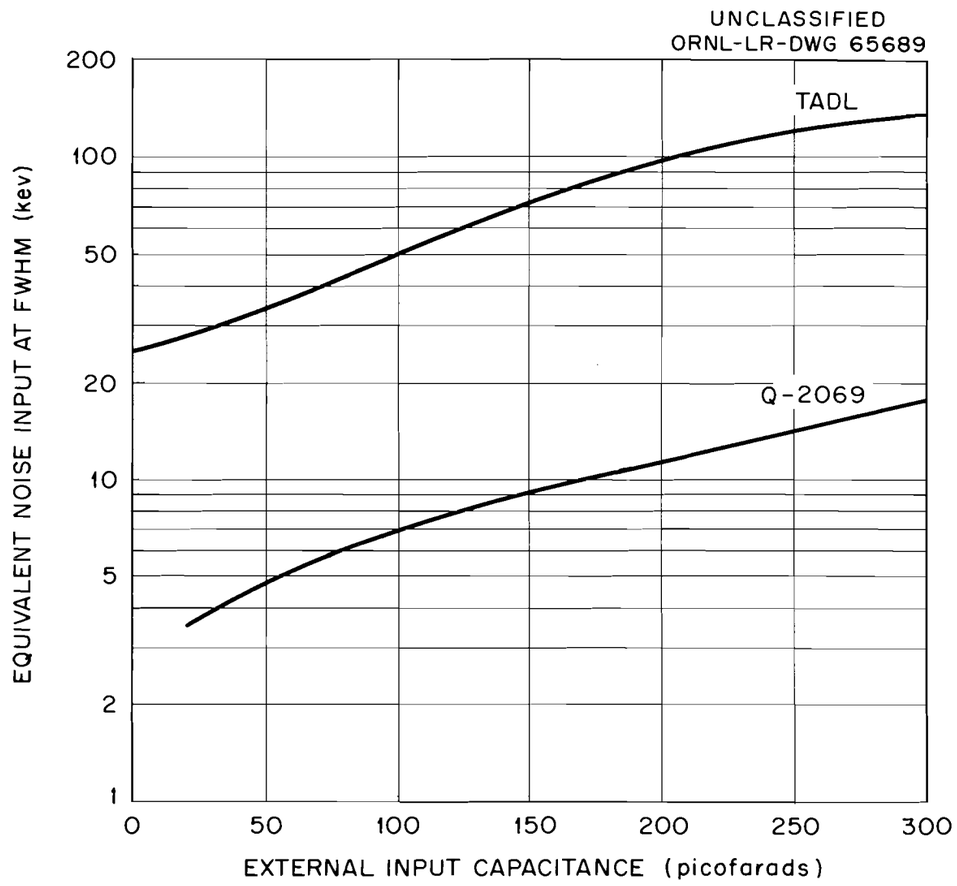
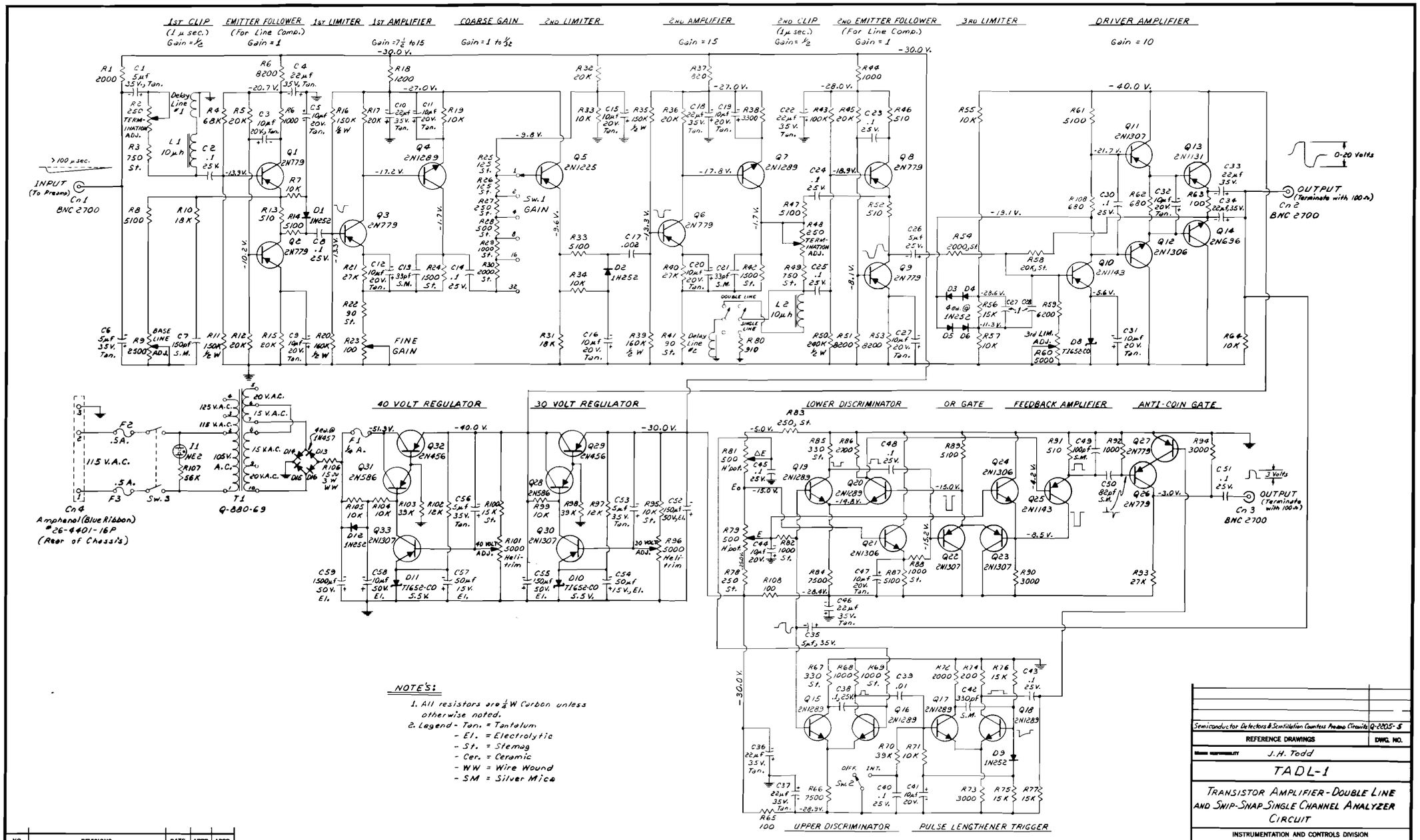


Fig. 1.27. Comparison of Resolution Spread Between the Transistor Amplifier – Double Line (TADL) and a Low-Noise Vacuum-Tube Amplifier (Q-2069). The TADL uses 2N779 transistors and the Q-2069 uses 417A/5842 tubes.



NOTES:

1. All resistors are 1/4 W Carbon unless otherwise noted.
2. Legend - Tan. = Tantalum
   - El. = Electrolytic
   - St. = Stemag
   - Cer. = Ceramic
   - WW = Wire Wound
   - SM = Silver Mica

NO.	REVISIONS	DATE	APPD	APPD

DRAWN E.C. Keith	DATE 7-10-61	SUBMITTED	DATE	APPROVED	DATE
DESIGNED T.L. Emmar	DATE	APPROVED	DATE	APPROVED	DATE
	DATE	APPROVED	DATE	APPROVED	DATE

Semiconductor Detectors & Scintillation Counters Preamp Circuits Q-2205-5

REFERENCE DRAWINGS — DWG. NO.

DESIGN RESPONSIBILITY J.H. Todd

TADL-1

TRANSISTOR AMPLIFIER-DOUBLE LINE AND SNIP-SNAP SINGLE CHANNEL ANALYZER CIRCUIT

INSTRUMENTATION AND CONTROLS DIVISION
OAK RIDGE NATIONAL LABORATORY
OPERATED BY
UNION CARBIDE NUCLEAR COMPANY

SUBMITTED — ACCEPTED — DATE — APPROVED — DATE

Q-2205-1

action of the feedback from the collector of Q1 to the base of Q2 and also from the collector of Q2 to the emitter of Q1 is to make the current in Q1 constant. Therefore, the output at the collector of Q2 is the difference between the emitter and base pulses at Q1. By proper adjustment of R9, the resistance losses in the delay line can be cancelled out.

The first limiter (D1) is a silicon diode, which conducts whenever the output pulse from Q2 exceeds 0.75 v. The output from D1 is limited to less than 1 v for input pulses of 4 v or less.

The first amplifier is a two-stage amplifier with negative feedback from the collector of Q4 to the base of Q3. Since the first stage is a PNP transistor and the second stage is an NPN transistor, both stages conduct more current during the negative input pulses. The maximum gain is 17.7, which equals (R24 + R22/R22), and the fine gain allows about a factor of two decrease in gain. Since the input pulses are limited by D1, the excessive saturation of Q4 is prevented, resulting in a fast recovery from overload.

With the coarse gain adjustment, the output of the first amplifier may be attenuated a maximum of 32 to 1. The attenuator output is coupled to an emitter-follower (Q5) that drives the second limiter and second amplifier. The output of the second amplifier, which is identical to the first amplifier except that the second amplifier carries higher emitter current in the second stage Q7, is used to drive the second delay line. By use of a switch, the second delay line may be removed; this gives a single-slipped, unipolarity pulse having a signal-to-noise ratio of about a factor of two better than for a double-clipped pulse. This lower noise ratio is useful when semiconductor detectors are used.

The second emitter-follower (Q8 and Q9) is used to compensate for losses in the second delay line, as described previously.

The output of the second emitter-follower is fed to the driver amplifier through a 2000-ohm resistor (R54). The driver amplifier consists of a single stage inverter (Q10) and a double, complementary emitter-follower (Q11, Q12, Q13, and Q14) from which the output is fed back to the input through the 20-kilohm resistor (R58). The gain of the stage is 10, which equals R58/R54. The driver amplifier can drive the output, terminated in 100 ohms, to ±10 v with 0.1% integral nonlinearity. Since the output is dc coupled to the input, potentiometer R60 adjusts the dc gain and, therefore, the dc level at the output.

The collector of Q10 is also connected to a series of biased diodes. When the output pulses exceeds ± 10 v in amplitude, these diodes conduct, shorting out the feedback and reducing the gain of the driver amplifier to less than unity for the time that the output pulses exceed ± 10 v. This diode network then acts as the third limiter. The potentiometer (R60) of the third limiter adjusts the dc level, as explained previously, so that the limitng action is symmetrical.

The power supply is double-regulated. Negative 40 v is supplied to the output stage, and the second regulator, which supplies negative 30 v to the other stages, acts as both a regulator for extra regulation and as a filter for the fast-rise, high-current pulses developed by the driver amplifier.

1.4 Preamplifier Circuit Description (Q-2205-5)

The preamplifier for scintillation counters consists of a triple emitter-follower (Q1, Q2, and Q3); the output impedance from the emitter-follower plus the 75-ohm resistor (R7) is used to terminate the output for the 100-ohm cable. The input impedance, which is about 1 megohm with a parallel capacity of 100 μμf (C2), is used to integrate the input signal. The main advantage of this circuit is that it works well at high counting rates.

The power for the preamplifier is supplied through the output cable and R8, and is regulated by a 12-v Zener diode (D1).

A pulser input, which can be used in parallel with the scintillation counter, is provided.

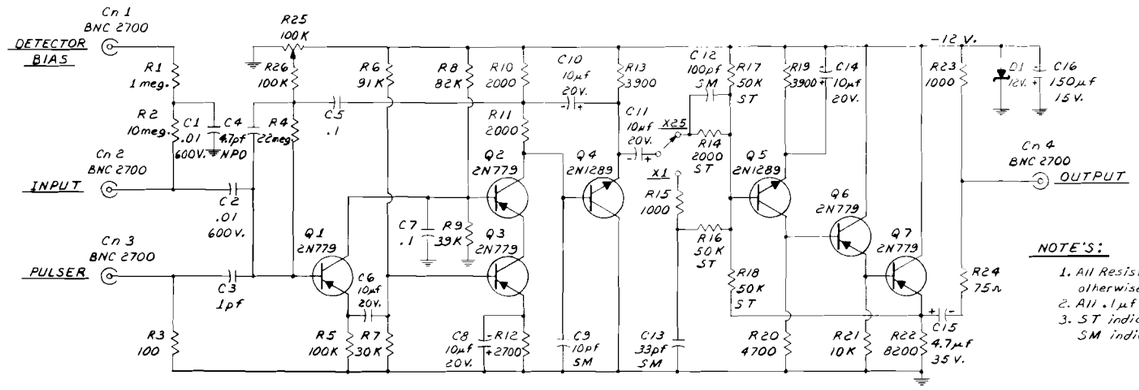
The preamplifier for semiconductor detectors has a "charge sensitive" input that consists of an emitter-follower (Q1) driving a bootstrapped cascode circuit (Q2 and Q3) with an emitter-follower output (Q4). The output is fed back to the input through the 100-μsec time constant (C4 and R4), which determines the charge gain of this stage and fall time of the output pulse. The charge gain of this stage is 1 mv per 100-kev energy loss in a silicon semiconductor detector. The bias potentiometer (R25) allows control of the base current of the input transistor and can be used to optimize the signal-to-noise ratio for different sizes of detectors.

An inverting amplifier with a low impedance output (Q5, Q6, and Q7) is used to further amplify the signal and drive the 100-ohm output cable. A choice of X1 or X25 gain is available by changing the feedback of this amplifier. The dc power for this preamplifier is supplied by the output cable, and dc regulation is provided by the 12-v Zener diode (D1).

1.5 Initial Testing

1. First check the power supplies and with only the power supply transistors installed, adjust the power supplies to their proper voltages.

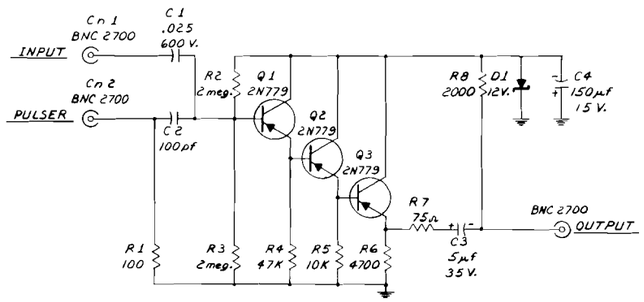
2. Test and insert transistors Q1 through Q9, and check voltages according to the circuit drawing. All transistors except Q5 should have a β of greater than 100 at I_e = 1 ma. Q5 should have a β of 35 or more.



NOTES:

1. All Resistors are ½ Watt Carbon unless otherwise noted.
2. All .1µf Capacitors are 25V. Ceramic.
3. ST indicates Stemag and SM indicates Silver Mica.

PREAMP FOR SEMICONDUCTOR DETECTORS



PREAMP FOR SCINTILLATION COUNTERS

NO.	REVISIONS			DATE	APPD	APPD
DRAWN E.C. Keith	DATE 11-14-61	SUBMITTED	DATE	APPROVED	DATE	
DESIGNED T.L. Emmer	DATE	APPROVED	DATE	APPROVED	DATE	
CHECKED T.L. Emmer	DATE	APPROVED	DATE	APPROVED	DATE	

Transistor Amplifier-Double Line & Snip-Snap Single Channel Analyzer Circuit — Q-2205-1

REFERENCE DRAWINGS — DWG. NO.

DESIGN RESPONSIBILITY: J. H. Todd

TADL-1

PREAMPS FOR SEMICONDUCTOR DETECTORS & FOR SCINTILLATION COUNTERS CIRCUITS

INSTRUMENTATION AND CONTROLS DIVISION
OAK RIDGE NATIONAL LABORATORY
OPERATED BY
UNION CARBIDE NUCLEAR COMPANY

SUBMITTED: T.L. Emmer | ACCEPTED | DATE | APPROVED: R.W. Hamming | DATE

Q-2205-5 RO

3. Select a transistor for Q10 having a β of 25 to 50 at I_e = 5 ma. For Q11 and Q12 select transistors that have β's matched to 10% and have a β greater than 100 at I_e = 1 ma. Also match the β's of Q13 and Q14 to 10%, with each having a minimum β of 25 at I_e = 5 ma.

4. Insert Q10 through Q14 and immediately adjust the collector voltage of Q10 to negative 19 v by adjusting the third limiter adjuster (R60).

5. With a preamplifier and mercury pulser, insert negative, 0.1-v pulses into the input, and adjust the termination adjuster (R2) and baseline adjuster (R9). The oscilloscope should be triggered by the pulse for all adjustments. The oscilloscope probe should be placed on the cathode of D1. Use a long sweep (100 μsec/cm) for adjusting R9.

6. Put the oscilloscope probe on the collector of Q4, and check the gain of the first amplifier and the fine-gain control.

7. With minimum fine gain, check the action of the first limiter by increasing the input pulse to about 4 v.

8. With the oscilloscope probe on the emitter of Q5, check the coarse gain.

9. With the oscilloscope probe on the cathode of D2, check the action of the second limiter.

10. Adjust the pulser so that the pulses at the cathode of D2 are 0.1 v. Check the gain of the second amplifier with the oscilloscope probe on the collector of Q7.

11. With the oscilloscope probe on capacitor C26 and the delay-line switch on double line, adjust the termination (R48).

12. Check the action of the delay-line switch.

13. With the oscilloscope probe on the output and the output terminated in 100 ohms, check the gain of the driver amplifier.

14. Increase the input pulses and check the action of the third limiter. Readjust the third limiter for symmetrical limiting.

15. With a 4-v input pulse and the oscilloscope probe on the output, readjust baseline adjuster (R9) for optimum.

16. Test and insert transistors in the Snip-Snap Single-Channel Analyzer as described in Section 2.4.

2.0 SNIP-SNAP SINGLE-CHANNEL ANALYZER

2.1 General Description

The Snip-Snap Single-Channel Analyzer, a companion unit to the TADL, acts as a crossover pick-off and has a fast, relatively jitter-free output which can be used in fast-coincidence experiments (Fig. 2.11). Both units are constructed on the same chassis.

The single-channel analyzer consists of a lower discriminator and an upper discriminator, whose outputs are in anticoincidence. When an input pulse triggers the lower discriminator, a feedback system, which is incorporated in the discriminator level control, changes the discriminator hysteresis so that the discriminator returns to the normal state as the input pulse changes polarity. An output pulse is generated when the discriminator returns to the normal state, so that the single-channel analyzer also acts as a crossover pickoff. The output pulse has sufficiently fast rise time for use in fast-coincidence experiments.

2.2 Specifications

1. Input: 0- to 10-v positive, double-delay-line clipped pulses.

2. E Dial Range: 0 to 10 v.

3. ΔE Dial Range: 0 to 10 v.

4. Output Pulse: 3-v positive pulse, 12-nanosec rise time, and 0.3-μsec width when terminated in 100 ohms.

5. Integral Nonlinearity: 0.1% with 0.1% nonlinearity potentiometers (0.5% potentiometers are normally supplied).

6. Time Shift of Output Pulse: less than 10-nanosec time shift for input pulses of 1- to 10-v amplitude and 0.1-μsec rise time (see Fig. 2.21).

2.3 Circuit Description (Q-2205-1)

The lower discriminator consists of an ac-coupled Schmitt trigger (Q19 and Q20); Q20 normally conducts 2 ma, as determined by the negative 15-v base voltage. This voltage, E_o, is supplied by the bleeder string through two complementary emitter-followers (Q21 and Q22) which compensate each other for effects of base-to-emitter voltage changes with temperature.

When the double-clipped input pulse, which is ac coupled to the base of Q19, exceeds the trigger level (E_o-E), Q19 conducts. The negative

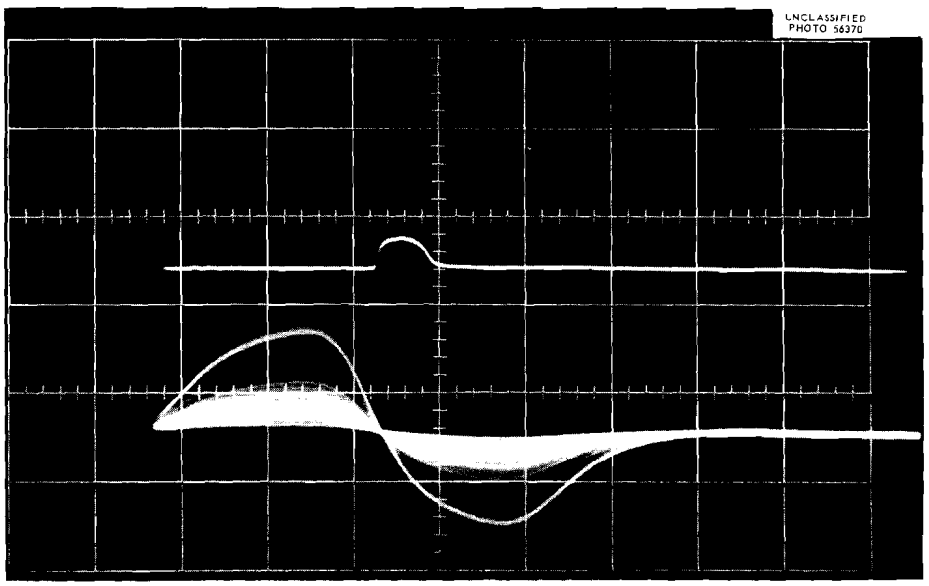


Fig. 2.11. Oscillogram Showing Output Pulses for Cs^{137} Gamma Rays from TADL (Top Wave) and from the Snip-Snap Single-Channel Analyzer (Bottom Wave). The horizontal scale is 0.5 μsec/cm and the vertical scale is 5 v/cm.

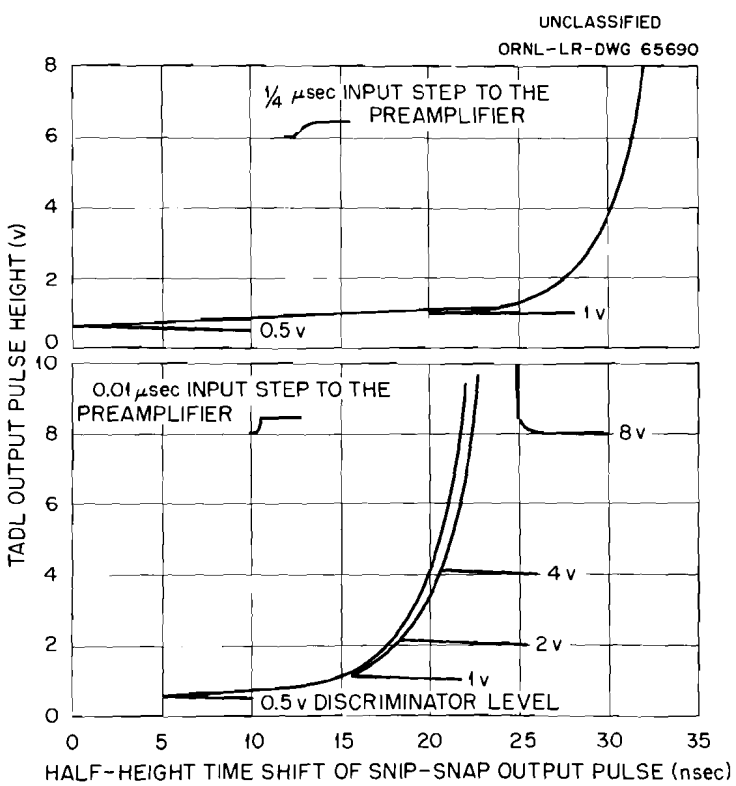


Fig. 2.21. Anti-Walk Characteristics of the Snip-Snap Single-Channel Analyzer.

pulse at the collector of Q19 is transmitted to the base of Q20 through emitter-follower Q22, causing Q20 to stop conducting. The positive pulse generated at the collector of Q20 then causes Q25 to stop conducting, and the collector voltage of Q25 drops until the clamp (Q24) starts to conduct. This negative pulse at the collector of Q25 is transmitted to the base of Q20 by emitter-follower Q23. Since the voltage at which the clamp transistor (Q24) starts conducting is E, the base of Q20 is now at voltage E, which is also the base-line voltage of the input pulse. Therefore, the lower discriminator will return to its normal state when the input pulse crosses the base line, regardless of where the discriminator level (E) is set.

When Q20 returns to its conducting state (the crossover point), the resulting negative pulse is transmitted to the anticoincidence gate through the emitter of Q25 and the differentiating network (C50 and R92). If the upper level discriminator has not triggered, Q27 is saturated and acts like a very low impedance. The negative pulse at the base of Q26 then drives Q26 into saturation, and since the collector voltage of Q26 is limited to 3 v, a positive 3-v output pulse is generated.

The upper discriminator consists of Q15 and Q16. Since the base of Q16 is at ΔE while the base of Q15 is at E, Q16 is normally conducting. When the input pulse exceeds ΔE-E, Q15 conducts and Q16 is cut off. The positive pulse generated at the collector of Q16 causes the pulse lengthener trigger (Q17 and Q18) to trigger, and a 2-μsec positive pulse is generated at the output of Q18. This positive pulse causes Q27 to stop conducting; therefore no current flows in Q26 when it is turned on by the negative pulse from the lower discriminator, and no output pulse is generated.

The upper discriminator can be switched off by Sw2, which drops the base voltage of Q17, so that the positive pulse from Q16 has insufficient amplitude to cause Q17 to conduct.

2.4 Initial Testing

1. Match the β of each trigger pair to 10% at I_e = 3 ma, with Q19 matched to Q20, Q15 matched to Q16, and Q17 matched to Q18. These transistors should have normal or less I_{co}.

2. Match the β of the four emitter-followers (Q21, Q22, Q23, and Q24) to 10% at I_e = 5 ma.

3. The β of Q25 should be greater than 40 at I_e = 3 ma.

4. Observe the output pulse for a 10-v input pulse from a TADL amplifier. Trigger the oscilloscope from the pulser that is used to drive the TADL preamplifier. There should be no observable shift of the output pulses as the E discriminator is varied from 0 to 10 v.

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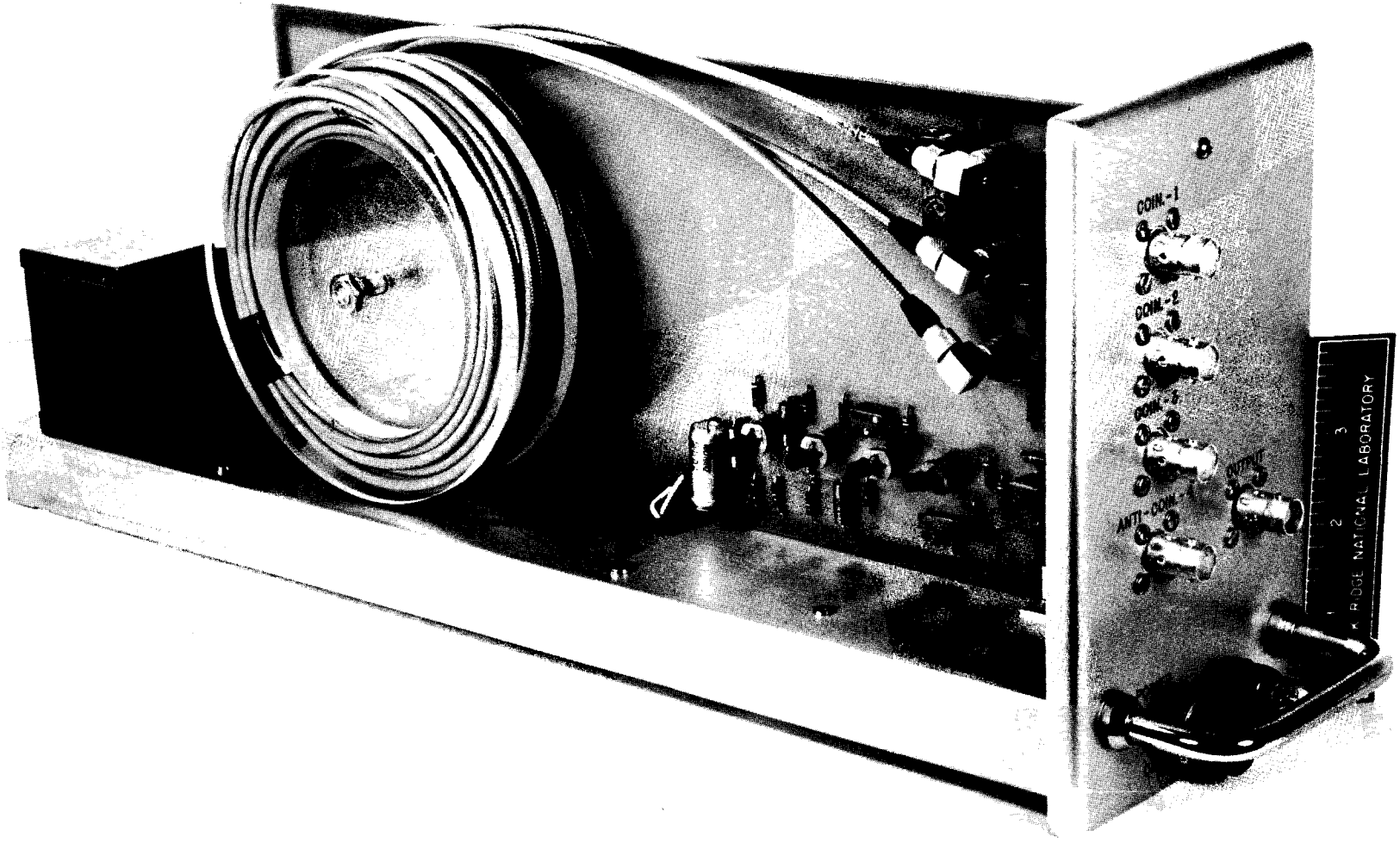


Fig. 3.11. Fast Coincidence Unit.

5. With E at maximum and a 10-v input, the base-to-emitter voltage of Q19 should not break down during the negative swing of the input pulse. Breakdown will show up on the emitter of Q19.

6. With E at 0 and ΔE at maximum, and with a 10-v input pulse, check for breakdown of Q15.

7. Check operation of the differential-integral switch.

3.0 FAST COINCIDENCE UNIT

3.1 General Description

The Fast Coincidence Unit (Fig. 3.11) was designed for use with Snip-Snap Single-Channel Analyzers in coincidence experiments. The single-channel analyzers determine the energy intervals of interest and generate output pulses which are used by the coincidence unit for determining the time coincidence of events in these energy intervals.

Miniature coaxial cables are used as shorted delay lines to shape the input pulses and determine the interval of time coincidence. The fast-coincidence unit can be used as a slow-coincidence unit when the delay lines are replaced with 100-ohm resistors and input pulses of the proper width are used. The cables are coiled at the back of the chassis and can be changed to suit the experiment. Three coincidence inputs and one anti-coincidence input are provided. For a double coincidence, one of the delay cables is disconnected.

Fast silicon diodes are used to determine the coincidence. The spectra of coincidence pulses are amplified and stretched by a biased amplifier, which increases the sensitivity, and used to trigger a one-shot multivibrator which generates the coincidence output pulse.

3.2 Specifications

1. Inputs: Snip-Snap Single-Channel Analyzer output pulses or any positive pulse greater than 1 v in amplitude. Input pulses must be wider than or equal to the coincidence time.

2. Coincidence Output: 3-v positive pulse of 1/2-μsec duration when terminated in 100 ohms.

3. Time Resolution: better than 1 nanosec for pulses having 12-nanosec or less rise time.

4. Coincidence Time: determined by the length of coaxial cable (cable delay is 1.6 nanosec/ft) or by the width of input pulses when 100-ohm resistors are substituted for the delay cables.

3.3 Circuit Description (Q-2213-1)

The shaper transistors (Q1, Q2, and Q3) normally conduct 30 ma. A positive input pulse (from a Snip-Snap Single-Channel Analyzer) to any channel will cause that transistor to stop conducting, and a negative current pulse will be generated at the collector of that transistor. Since this current pulse appears across a terminated, shorted delay line, a negative-voltage pulse will be generated, which has a width of twice the delay time of the cable.

If positive pulses to each coincidence input arrive within a time interval such that all delay lines have a negative pulse across their termination, the coincidence diodes (D1, D2, and D3) are cut off, and a negative pulse is generated at the base of Q5. If this negative pulse is of sufficient amplitude to overcome the bias voltage (determined by the bleeder string, R22, R23, and R24), biased amplifier Q5 conducts. If the positive pulse generated at the collector of Q5 is of sufficient amplitude, the coincidence trigger (Q6 and Q7) is triggered and a negative pulse of 1/2-μsec duration is generated at the collector of Q7. This pulse drives Q8 into saturation, and a 3-v positive output pulse is generated.

3.4 Initial Testing

1. With only the power supply transistors installed, check the power supply and adjust the supply voltage to negative 12 v.

2. Select those transistors having a β of 30 or more at I_e = 10 ma for use as Q1, Q2, and Q3. Install these transistors and check their emitter and collector voltages.

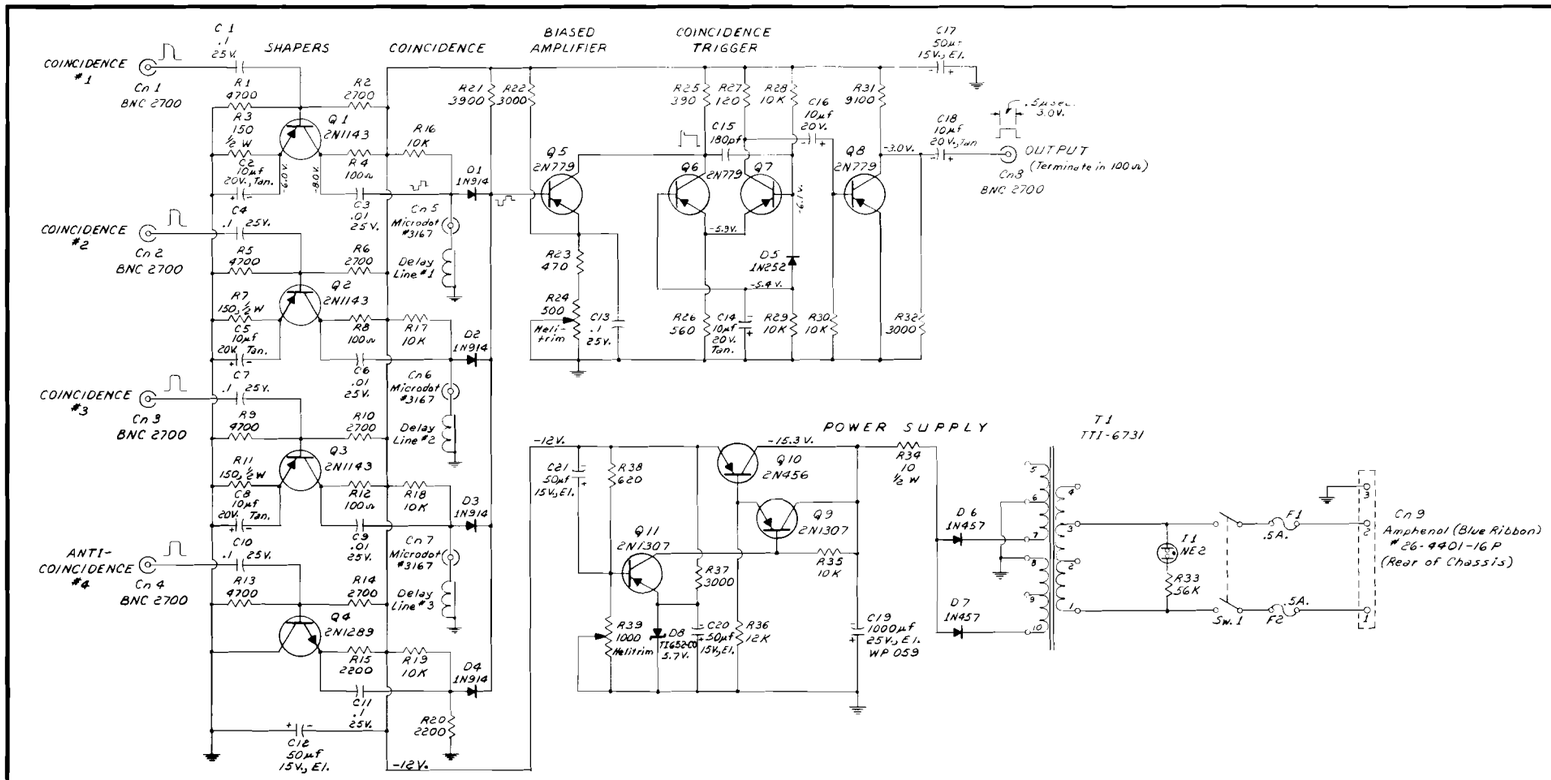
3. Select for the other transistors those having a β of greater than 80 at I_e = 1 ma, and install.

4. Check the voltages in the rest of the circuit.

5. Install the shorted delay lines.

6. Connect the output of the Snip-Snap Single-Channel Analyzer to all three coincidence inputs, and adjust the biased amplifier adjustment (R24) until an output pulse is observed.

7. When one of the input leads is disconnected, the coincidence output pulse should disappear. Check all inputs for this condition.



NOTE'S:

1. All resistors are ¼ W Carbon unless otherwise noted.
2. All Delay Lines are Microdot 93-3908, 25 Feet long for 80 nano second clipping time. For double coincidence, disconnect unused Delay Line.
3. Legend - El. = Electrolytic Capacitor
   Tan. = Tantalytic Capacitor.

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CHECKED	DATE	APPROVED	DATE	APPROVED	DATE	

Printed Circuit Board — Q-2213-2

REFERENCE DRAWINGS — DWG. NO.

DESIGN RESPONSIBILITY J.H. Todd

FAST COINCIDENCE FOR TADL-1

CIRCUIT

INSTRUMENTATION AND CONTROLS DIVISION
OAK RIDGE NATIONAL LABORATORY
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Q-2213-1 RO

8. Connect the output from the Snip-Snap Single-Channel Analyzer to the anticoincidence input. The coincidence output pulse should then disappear.

4.0 BIASED AMPLIFIER AND LINEAR GATE

4.1 General Description

When a pulse-height analyzer is used to accumulate spectra from semiconductor detectors, the analyzer channels are often too wide to provide an adequate display of these spectra. A biased amplifier overcomes this difficulty by providing facilities for a large zero offset (bias level) and postamplification of the spectra above the bias level.

This biased amplifier, Fig. 4.11, has two cascaded, biased amplifier stages. When the input pulse exceeds the bias level, that portion exceeding the bias level is amplified by the first biased amplifier and used to turn on the second biased amplifier, from which the output is fed back to the first biased amplifier. Once the feedback is applied, the output is linear with respect to the input. By varying the feedback, a postgain of 1 to 16 can be obtained.

In the linear-gate mode of operation, the first biased amplifier output is clamped by a one-shot multivibrator. When a gate trigger-pulse arrives, the one-shot multivibrator is triggered and the clamp released. The biased amplifier then operates as normal.

4.2 Specifications

1. Input: 0- to 10-v positive pulses.
2. Gate Trigger: 3-v positive pulse.
3. Bias Level: 0 to 10 v.
4. Post Gain: 1, 2, 4, 8, and 16.
5. Output: 0- to 10-v positive pulses into 100 ohms.
6. Integral Nonlinearity: 0.5% for either bias level or output pulse.
7. Stability: 0.5 mv/^{o}C times the post gain.

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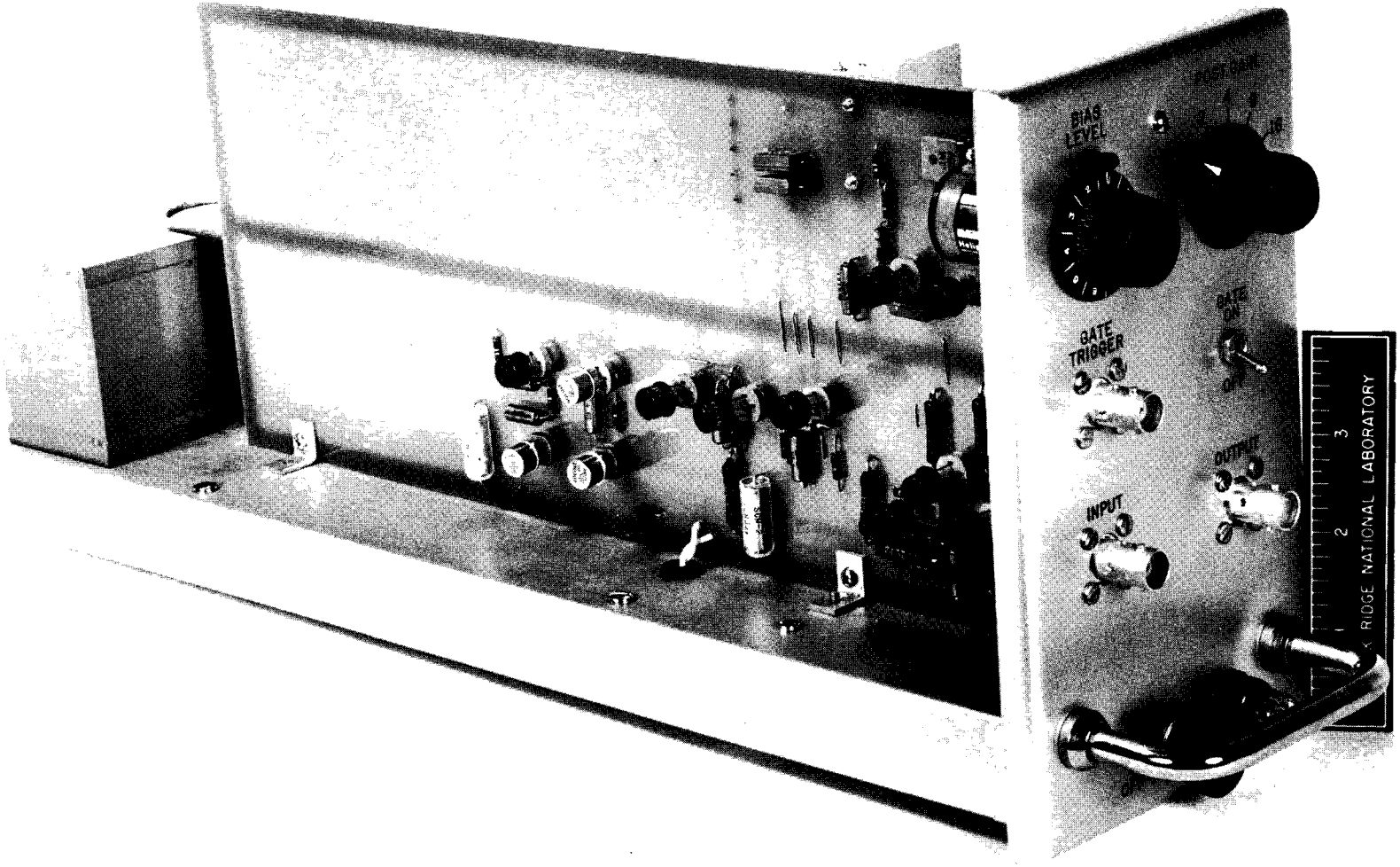


Fig. 4.11. Biased Amplifier and Linear Gate.

4.3 Circuit Description (Q-2238-1)

The first biased amplifier consists of Q10 and Q11. Q11 is normally conducting, and Q10 is cut off by a voltage determined by the bias level. The collector current of Q11 is divided equally between R30 and the clamp transistor Q9. When a positive input pulse exceeds the bias level, the current in Q10 increases until Q10 has about the same current as Q11. Then the current through Q9 is zero, and the collector of Q11 rises.

This positive pulse is applied to the second biased amplifier (Q13 and Q14) by the emitter-follower (Q12). Since Q13 is normally cut off, the positive input pulse causes Q13 to conduct, and negative feedback is applied to the base of Q11 through the feedback network. The action of the feedback is to tend to make the base of Q11 follow the input pulse, and therefore the emitter of Q13 also follows the input pulse at an amplified level. This biased, amplified pulse is applied to the output through the double, complementary emitter-follower (Q15, Q16, Q17, and Q18).

When the unit is in the linear-gate mode, Q8 is conducting and its collector current flows through clamp Q9. Therefore, the collector of Q11 cannot rise until this current is removed. Since Q8 is part of a one-shot multivibrator (Q7 and Q8), a positive gate-trigger pulse will cause Q7 to conduct and remove the clamp current. The biased amplifier will then operate exactly the same as in the nongating mode just described.

4.4 Initial Testing

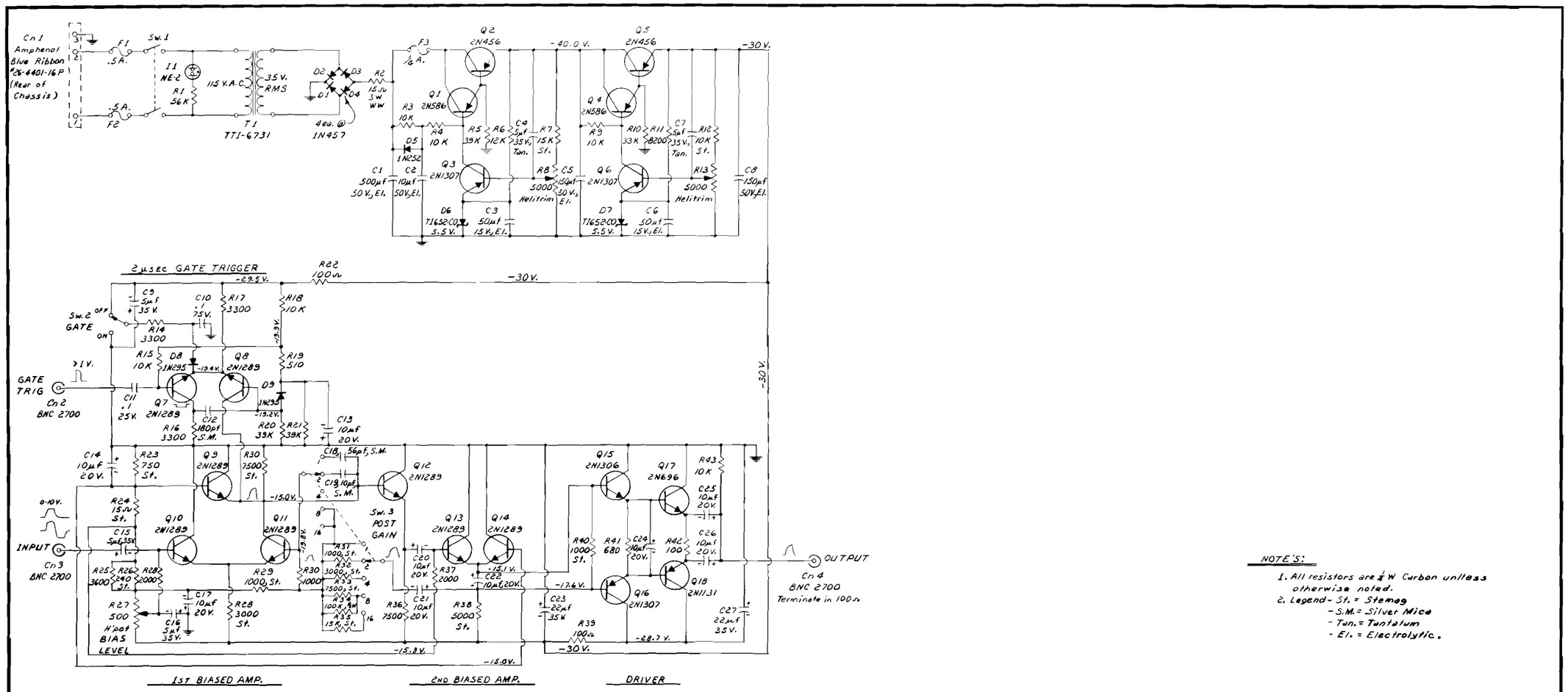
1. Test the transistors in the power supply for a β greater than 50 at $I_e = 1$ ma.

2. Install the power supply transistors and adjust the negative 40-v and negative 30-v regulators.

3. Test the other transistors and install. All these transistors should have a β of greater than 100 at $I_e = 1$ ma, except Q17 and Q18 which should have a β of greater than 25. These transistors should be matched for β: Q8 to Q9, Q10 to Q11, Q13 to Q14, Q15 to Q16, and Q17 to Q18.

4. Using pulses from the TADL and triggering the oscilloscope from the pulse generator used to drive the TADL, check the operation of the bias level and post-gain switch.

5. Connect the positive (plus gate main sweep) pulse from the oscilloscope to the gate-trigger input through a 20-picof series capacitor. Check the action of the gate trigger.



NOTES:

1. All resistors are 1/4 W Carbon unless otherwise noted.
2. Legend - St. = Stemag
   - S.M. = Silver Mica
   - Tan. = Tantalum
   - El. = Electrolytic.

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SUPERVISED	DATE	APPROVED	DATE	APPROVED	DATE	

REFERENCE DRAWINGS	DWG. NO.
DESIGN RESPONSIBILITY J. H. Todd	

BIASED AMPLIFIER & LINEAR GATE

CIRCUIT

INSTRUMENTATION AND CONTROLS DIVISION
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